WHAT IS CLAIMED IS:

1. A method of fabricating a MOSFET device, comprising the steps of:

providing a substrate, the substrate including an active region and a non-active region;

forming a plurality of trenches;

forming a dielectric layer in the trenches;

removing the dielectric layer in the trenches of the active region;

forming a thin insulating layer in the trenches of the active region and over the substrate;

forming a conducting layer in the trenches of the active region and over the substrate;

patterning the conducting layer to form a gate layer;

implanting the substrate with first ions; and

implanting the substrate with second ions by using a mask, wherein the mask exposes the trenches of the active region, and the opening of the mask is wider than the trench.

2. A method according to claim 1, wherein the dielectric layer is formed by CVD.

3. A method according to claim 1, wherein the thin oxide layer is formed by thermal oxidation.

4. A method according to claim 1, wherein the thickness of the thin oxide layer is about 0.1μm.

5. A method according to claim 1, wherein the conducting layer is formed by CVD.

6. A method according to claim 1, wherein said step of implanting the substrate with first ions is to form a shallow doped region.

7. A method according to claim 1, wherein said step of implanting the substrate with second ions is to form a deep doped region.

8. A MOSFET device, comprising:

a substrate, wherein the substrate includes an active region and a non-active region, and the substrate includes a plurality of trenches;

a plurality of shallow trench isolation structures, wherein the shallow trench isolation structures are in the trenches of the non-active region;

a thin insulating layer, formed in the trenches of the active region and over the surface of the substrate;

a multiple T-shaped gate layer, including a first part and a second part, wherein the first part is on the surface between two trenches, and the second part is in the trenches

of the active region; and

a source/drain region, including a shallow doped region and a deep doped region, wherein the shallow doped region is in the substrate under the first part, and the deep doped region is in the substrate besides the second part;

wherein the deep doped region is deeper than the trenches, and the trenches are deeper than the shallow doped region.

9. A MOSFET device according to claim 1, wherein the thin insulating layer on side-walls of the trenches is about 0.1μm.

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